REMARKS

The present application was filed on July 23, 2001 with claims 1-29. In the outstanding Office Action dated July 3, 2002, the Examiner: (i) withdrew from consideration claims 18-25 as being drawn to a non-elected invention; (ii) rejected claims 1-17 and 26-29 under 35 U.S.C. §112, second paragraph; (iii) rejected claims 1, 2, 6-9, 13-16 and 26-29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,912,054 to Tomassetti (hereinafter "Tomassetti"); and (iv) rejected claim 17 under 35 U.S.C. §103(a) as being unpatentable over Tomassetti.

In this response, Applicant affirms the election of group II claims (claims 1-17 and 26-29) by canceling claims 18-25 without prejudice. Claims 1 and 26 have been amended and claims 30 and 31 have been added. Additionally, Applicant traverses the §112, §102(b) and §103(a) rejections. Applicant respectfully requests reconsideration of the present application in view of the above amendments and the following remarks.

Claims 1-17 and 26-29 stand rejected under §112, second paragraph as being indefinite for "failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention" (present Office Action; page 2, paragraph 3). Specifically, the Examiner contends that with regard to claims 1 and 26, the recitation of "... electrical isolation between the first and second circuit sections is increased" in these claims is "vague because it cannot be determined how the phrase further defines the claimed subject matter. It is not known how the circuit sections, which are already isolated, can be more isolated" (present Office Action; page 2, last paragraph to page 3, paragraph 1). Accordingly, claims 1 and 26 have been amended in a manner which Applicant believes addresses the Examiner's §112 rejection of these claims.

Applicant respectfully traverses the §112 rejection of claim 2. With regard to claim 2, the Examiner contends that the recitation of "conductive plugs" in the claim "may not be given a meaning repugnant to the usual meaning of that term" (present Office Action; page 3, paragraph 2). The Examiner further contends that "The term 'conductive plugs' in claim 2 is used by the claim to mean 'low-resistance diffusion region' while the accepted meaning is 'a conductive plug, such as metal or polysilicon'" (present Office Action; page 3, paragraph 2). Applicant respectfully disagrees

with the Examiner's contention. A "plug," as the term is typically used, may be defined as "a piece used to fill a hole" *(Webster's Ninth New Collegiate Dictionary*, Merriam-Webster, Inc., 1991). The term "conductive" may be defined as "the quality or power of conducting or transmitting," as in an electrical current *(Webster's Ninth New Collegiate Dictionary*, Merriam-Webster, Inc., 1991). Although conductive plugs may generally be formed of metal or polysilicon material, as the Examiner states, conductive plugs are not limited to those materials. Rather, any electrically conductive material, including, for example, diffused low-resistance n^+ material, may be used to form a conductive plug, as in an illustrative embodiment of the present invention (Specification; page 12, lines 16-20). Thus, Applicant submits that the meaning of the term "conductive plug," as recited in claim 2, is not repugnant to the usual meaning of that term. Accordingly, withdrawal of the §112 rejection of claim 2 is respectfully solicited.

Claims 1, 2, 6-9, 13-16 and 26-29 stand rejected under §102(b) as being anticipated by the Tomassetti reference. Specifically, with regard to independent claim 1, and independent claim 26 which is of similar scope, the Examiner contends that Tomassetti teaches an integrated circuit comprising "a first circuit section (18, 20) formed in a substrate; a second circuit section (16) formed in the substrate . . . an isolation buried layer (13) formed under at least a portion of the first circuit section; and a conductive layer (78) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer" (present Office Action; page 3, paragraph 4). The Examiner acknowledges that Tomassetti "does not explicitly teach the conductive layer reducing an effective lateral resistance of the isolation buried layer" (present Office Action; page 4, paragraph 2). However, the Examiner further contends that the device taught by Tomassetti "would have inherently performed the same function since Tomassetti teaches each and every structural limitation of the claimed invention" (present Office Action; page 4, paragraph 2).

While Applicant respectfully disagrees with the Examiner's contentions, claims 1 and 26 have been amended to clarify the claimed invention. Specifically, claim 1, as amended, requires that the conductive layer be coupled to the isolation buried layer "at a plurality of points spaced throughout the buried layer." The Tomassetti reference fails to teach or suggest this limitation. Rather, Tomassetti discloses deep diffusions (32) forming an isolation ring surrounding, and in

electrical contact with, a buried layer (13) (Tomassetti; column 3, lines 48-61). In contrast to the claimed invention, Tomassetti further teaches that connection to the buried layer is made at a single point, stating that "the isolation ring 32 has formed therein an electrical contact 78" (Tomassetti; column 4, lines 59-60; FIG. 1).

Applicant submits that the lateral (i.e., sheet) resistance of a buried layer cannot be adequately reduced by making connection to a conductor formed on the surface of the integrated circuit via a single point, as taught by Tomassetti. Thus, the arrangement taught by Tomassetti does not inherently reduce the effective lateral resistance of the buried layer, as the Examiner contends (present Office Action; page 4, paragraph 2). However, this is not a concern for Tomassetti since Tomassetti is not directed to increasing isolation in an integrated circuit by reducing the effective lateral resistance of the buried layer, as in the claimed invention. Instead, Tomassetti relates to "techniques for biasing integrated bipolar-CMOS semiconductor circuits utilizing different operating voltages" (Tomassetti; column 1, lines 12-14).

Inasmuch as Tomassetti fails to teach or suggest a conductive layer formed on the surface of the integrated circuit that is coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, as required by claims 1 and 26 as amended, Applicant respectfully submits that claims 1 and 26 are patentable over the Tomassetti reference. Accordingly, favorable consideration and allowance of claims 1 and 26 are respectfully solicited.

With regard to claims 2, 6-9 and 13-16, which depend from claim 1, and claims 27-29, which depend from claim 26, Applicant respectfully asserts that these claims are also patentable over the prior art by virtue of their dependency from their respective independent claims, which are believed to be patentable for at least the reasons set forth above. Moreover, these claims define additional patentable subject matter in their own right. For example, claim 3 further defines the conductive layer as comprising "a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net." Tomassetti fails to teach or suggest this feature of claim 3. Therefore, claims 2, 6-9, 13-16 and 27-29 are believed to be patentable over the cited prior art, not merely by virtue of their dependency from claims 1 and 26, respectively, but also in their own

right. Accordingly, favorable reconsideration and allowance of these claims are respectfully requested.

Claim 17 stands rejected under §103(a) as being unpatentable over Tomassetti. Specifically, the Examiner acknowledges that "Tomassetti does not teach the isolation buried layer is formed in the substrate at dept in a range from about 2 micrometers to about 5 micrometers from an upper surface of the substrate" (present Office Action; page 6, paragraph 1). However, the Examiner contends that it would have been obvious to a person having skill in the art "to find the optimal depth of the buried layer through routine experimentation" (present Office Action; page 6, paragraph 1). Applicant respectfully disagrees with this contention and submits that claim 17 is also patentable over the prior art by virtue of its dependency from claim 1, which is believed to be patentable for at least the reasons set forth above. Moreover, claim 17 defines additional patentable subject matter in its own right. In this regard, Applicant asserts that Tomassetti fails to teach or suggest forming the isolation buried layer at a depth in the range of about 2 micrometers to about 5 micrometers, as required by claim 17, since it would be impracticable to form a conventional buried layer at a depth in this range. Therefore, claim 17 is believed to be patentable over the cited prior art, not merely by virtue of its dependency from claim 1, but also in its own right. Accordingly, favorable reconsideration and allowance of claim 17 are respectfully solicited.

With regard to newly presented claims 30 and 31, Applicant respectfully asserts that these claims are patentable over the Tomassetti reference since, as previously stated, Tomassetti fails to teach or suggest a conductive layer formed as "a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net," as required by claim 30. Furthermore, Tomassetti fails to teach or suggest first and second conductive layers formed on the surface of the integrated circuit wherein "at least one of the first conductive layer and the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net," as recited in claim 31. Accordingly, Applicants assert that claims 30 and 31 are patentable over the prior art of record. Favorable consideration and allowance of these claims are therefore respectfully requested.

In view of the foregoing, Applicant believes that claims 1-17 and 26-29 as amended, as well as newly presented claims 30 and 31, are in condition for allowance, and respectfully requests withdrawal of the §112, §102(b) and §103(a) rejections.

Attached hereto is a marked-up version of the changes made to the claims by the present Amendment. The attachment is captioned "Version with Markings to Show Changes Made."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 18-25 have been canceled without prejudice.

Claims 1 and 26 have been amended by rewriting same as follows:

1. (Amended) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer[, whereby] to thereby increase an electrical isolation between the first and second circuit sections [is increased].

26. (Amended) A semiconductor device formed on a semiconductor wafer, comprising:

a first circuit section formed in a substrate of the semiconductor wafer;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the semiconductor wafer and electrically coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer[, whereby] to thereby increase an electrical isolation between the first and second circuit sections [is increased].

The following new claims have been added:

--30. (New) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer;

wherein the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.--

--31. (New) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

a first isolation buried layer formed under at least a portion of the first circuit section;

a first conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the first isolation buried layer;

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer;

wherein at least one of the first conductive layer and the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.--